Patent claims

1. A method in a telecommunication or data communication network of reducing phase jumps in a frame synchronisation signal when switching from a first original reference signal to a second reference signal,
characterized in

generating a first and a second master reference signal phase locked to the first and the second original reference signal, respectively, each with a frequency n times the frequency of the corresponding original reference signal,

selecting one of the master reference signals by a selection signal,

dividing the frequency of the selected master reference signal back to the frequency of its corresponding reference signal,

inputting the frequency divided signal into a Phase-Locked Loop circuit for generating the frame synchronisation signal.

2. Method according to claim 1,
characterized in that in the selection step the first master reference signal is selected when the selection signal is low, and the second master signal is selected when the selection signal is high, or vice versa.

3. Method according to claim 1 or 2,
characterized in that the dividing step is carried out by counting the number of periods of the selected master reference signal and outputting a pulse like in the corresponding original reference signal for each nth period of the selected master reference signal.

4. Method according to one of the preceding claims, characterized in that the periods of the master reference signal are longer than the delta period of maximum tolerable frequency deviation of the corresponding original reference signal.

5. Method according to one of the preceding claims, characterized in that the frame synchronisation signal is a master frame synchronisation signal in a PDH system.

6. An arrangement in a node of a telecommunication or data communication network of reducing phase jumps in a frame synchronisation signal when switching from a first original reference signal to a second reference signal, characterized in

an element for each original reference signal generating a first and a second master reference signal phase locked to the first and the second original reference signal, respectively, each with a frequency n times the frequency of the corresponding original reference signal,

a multiplexer with the first and the second master reference signal as input in addition to a selection signal selecting one of the master reference signals as the output of the multiplexer,

a divider dividing the frequency of the output of the multiplexer back to the frequency of the corresponding reference signal,

a Phase-Locked Loop circuit for generating the frame synchronisation signal having the divider output signal as input.

7. Arrangement according to claim 6, characterized in that the multiplexer selects the first master reference signal when the selection signal is low, and the second master signal when the selection signal is high, or vice versa.

8. Arrangement according to claim 6 or 7, characterized in that the divider is a counter counting the number of periods of the output signal of the multiplexer outputting a pulse like in the corresponding original reference signal for each nth period of the output signal of the multiplexer.

9. Arrangement according to one of the claims 6-8, characterized in that the periods of the master reference signals are longer than the delta period of maximum tolerable frequency deviation of the corresponding original reference signal.

10. Arrangement according to one of the claims 6-9, characterized in that the node is a switch.

11. Arrangement according to one of the claims 6-10, characterized in that the frame synchronisation signal is a master frame synchronisation signal in a PDH system.